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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/721,984 | 11/25/2003 | Mukta G. Faroog | END920030114US1 | 6936 |

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| EXAMINER | |
|---|---|
| WILLIAMS, ALEXANDER O | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 06/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Offic Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/721,984 | FAROOG ET AL. | |
| | Examiner | Art Unit | |
| | Alexander O. Williams | 2826 | |

*-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --*

**Period f r Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Pri rity under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/721984 Attorney's Docket #: END920030114US1
Filing Date: 11/25/2003;

Applicant: Farooq et al.

Examiner: Alexander Williams

Applicant's Amendment filed 3/14/06 to the election with traverse of species I, figure 2, claims 1-20, filed 10/27/05, has been acknowledged.

Claims 1 to 20 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1, 10 and 16, it is unclear and confusing to what is meant by "an interposer having a **connection only** to the **semiconductor chip** and to **the substrate**. This claim language is not correct because the interposer connects to the bump before it connects to the semiconductor chip and an electrical element before it connects to the substrate.

Any of claims 1 to 20 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

**(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.**

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-3, 6-8, 10, 11, 13, 14, 16-18 and 20 are rejected under 35 U.S.C. § 102(b) as being anticipated by Jacobs (U.S. Patent # 6,294,407 B1).

1. Jacobs (figures 1 to 13) specifically figure 13 show a semiconductor module **1300**, comprising: a semiconductor chip **102'**; a substrate **120**; and an interposer structure **1400** having a connection only to the semiconductor chip and to the substrate, wherein the interposer structure includes an elastomeric compliant material having metallurgical **114** through connections having a predetermined shape, wherein the metallurgical through connections form the connection.

2. The semiconductor module of claim 1, Jacobs show wherein the elastomeric, compliant material has the metallurgical through connections being one of the group consisting of: embedded and positioned therein.
3. The semiconductor module of claim 1, Jacobs show wherein the predetermined shape is selected from the group consisting of spherical, elongate, c-shaped, s-shaped and ellipsoid.
6. The semiconductor module of claim 1, Jacobs further comprising underfill **106** for sealing the interposer structure between the semiconductor chip and the substrate.
7. The semiconductor module of claim 1, Jacobs show wherein the metallurgical through connections of the interposer structure electrically connect an under bump metallization **104** of the semiconductor chip to a top surface metallization of the substrate.
8. The semiconductor module of claim 7, Jacobs show wherein the metallurgical through connections are soldered to at least one of the under bump metallization **104** or the top surface metallization.
10. Jacobs (figures 1 to 13) specifically figure 13 show a semiconductor module **1300**, comprising: a semiconductor chip **102'** having an under bump metallization **104**; a substrate **120** having a top surface metallization; and an interposer structure **140** only in contact with the under bump metallization and the top surface metallization, wherein the interposer structure comprises an elastomeric, compliant material that includes metallurgical through connections having a predetermined shape.
11. The semiconductor module of claim 10, Jacobs show wherein the predetermined shape is selected from the group consisting of spherical, elongate, c-shaped, s-shaped and ellipsoid.
13. The semiconductor module of claim 10, Jacobs further comprising underfill **106** for sealing the interposer structure between the semiconductor chip and the substrate.
14. The semiconductor module of claim 10, Jacobs show wherein the metallurgical through connections are soldered to at least one of the under bump metallization or the top surface metallization.

16. Jacobs (figures 1 to 13) specifically figure 13 show a method for forming a semiconductor module **1300**, comprising: embedding metallurgical **114** through connections within an elastomeric, compliant material to form an interposer structure **140**; and positioning the interposer structure between a semiconductor chip **102'** and a substrate **120** to electrically connect and only contact the semiconductor chip to the substrate.

17. The method of claim 16, Jacobs show wherein the metallurgical **114** through connections electrically connect an under bump metallization **104** of the semiconductor chip to a top surface metallization of the substrate.

18. The method of claim 17, Jacobs further comprising soldering the interposer structure to at least one of the under bump metallization or the top surface metallization.

20. The method of claim 16, Jacobs further comprising sealing the interposer structure between the semiconductor chip and the substrate with underfill **106**.

[0108] The PGP also can enable area array solder bumping of components on a low density PCB by transformation of geometry and by providing solder bump compatible surface metallurgy and/or solder itself. The PGP can serve as stress relieving structure between a substrate and an electronic component if elastomeric materials are utilized. For example, a layer of elastomeric material may be interposed between the PCB and the decal to provide stress relief. This can further enable an area array flip-chip.

Claims 1-3, 7-11 and 14-18 are rejected under 35 U.S.C. § 102(e) as being anticipated by Pierson et al. (U.S. Patent # 6,774,315 B1).

1. Pierson et al. (figures 1 to 10) specifically figure 8 show a semiconductor module, comprising: a semiconductor chip **23**; a substrate **33**; and an interposer structure **1,3** having a connection only to the semiconductor chip and to the substrate, wherein the interposer structure includes an elastomeric compliant material having metallurgical **25,29,5** through connections having a predetermined shape, wherein the metallurgical through connections form the connection.

2. The semiconductor module of claim 1, Pierson et al. show wherein the elastomeric, compliant material has the metallurgical through connections being one of the group consisting of: embedded and positioned therein.

3. The semiconductor module of claim 1, Pierson et al. show wherein the predetermined shape is selected from the group consisting of spherical, elongate, c-shaped, s-shaped and ellipsoid.

7. The semiconductor module of claim 1, Pierson et al. show wherein the metallurgical through connections of the interposer structure electrically connect an under bump metallization **25** of the semiconductor chip to a top surface metallization of the substrate.

8. The semiconductor module of claim 7, Pierson et al. show wherein the metallurgical through connections are soldered to at least one of the under bump metallization **25** or the top surface metallization.

9. The semiconductor module of claim 1, Pierson et al. show wherein the metallurgical **29** through connections are coated with gold.

10. Pierson et al. (figures 1 to 10) specifically figure 8 show a semiconductor module, comprising: a semiconductor chip **23** having an under bump metallization **25**; a substrate **33** having a top surface metallization; and an interposer structure **1,3** only in contact with the under bump metallization and the top surface metallization, wherein the interposer structure comprises an elastomeric, compliant material that includes metallurgical through connections having a predetermined shape.

11. The semiconductor module of claim 10, Pierson et al. show wherein the predetermined shape is selected from the group consisting of spherical, elongate, c-shaped, s-shaped and ellipsoid.

14. The semiconductor module of claim 10, Pierson et al. show wherein the metallurgical through connections are soldered to at least one of the under bump metallization or the top surface metallization.

15. The semiconductor module of claim 1, Pierson et al. show wherein the metallurgical **29** through connections are coated with gold.

16. Pierson et al. (figures 1 to 10) specifically figure 8 show a method for forming a semiconductor module, comprising: embedding metallurgical **5,25,29** through connections within an elastomeric, compliant material to form an interposer structure **3,1**; and positioning the interposer structure between a semiconductor chip **23** and a substrate **33** to electrically connect and only contact the semiconductor chip to the substrate.

17. The method of claim 16, Pierson et al. show wherein the metallurgical through connections electrically connect an under bump metallization **25** of the semiconductor chip to a top surface metallization of the substrate.

18. The method of claim 17, Pierson et al. further comprising soldering the interposer structure to at least one of the under bump metallization or the top surface metallization.

[0028] With reference to FIG. 1, there is shown an interposer arrangement, in partial cross-section, fabricated in accordance with the present invention. Interposer 1 is fabricated from a flexible dielectric layer 3 of low modulus material such as, for example, Rogers 2800 material, Dow 1-4173 material or GE 3281 material. Layer 3 may have an elastic modulus in the range of about 50,000 psi to about 400,000 psi. The thickness of flexible dielectric layer 3 may range between 10 to 15 mils. This may be obtained by laminating several layers of Rogers 2800 material, for example, with heat and pressure to form this thickness. An array of vias 5 are formed in the layer, each approximately 2 mils in diameter. These vias may be fabricated by laser ablation, for example. The array of vias are patterned to match the pattern of connection points on the flip chip die and corresponding connection points on the circuit card chip carrier to which it will be interposed and connected. The vias are then copper plated to form copper walls 6. This may be achieved by first plating all of layer 3 with electroless copper. A plating resist is then applied to the vias and both sides of the layer. A mask is aligned to retain resist in the vias and at sites surrounding the end of the vias so as to form top pads 7 and bottom pad 9 at the respective ends of the copper walls. Each pad may be approximately 4 mils in diameter. The resist is then exposed and developed and exposed copper on both sides removed after which the resist is stripped off. Further plaiting may then be carried out. For some applications, the copper plated vias could then be filled with a conductive

adhesive composition, if necessary, but the arrangements shown in FIGS. 5 and 7 use a different approach.

[0029] It should be understood that although in the various embodiments described herein, reference is made to use of copper to form the walls and pads, it is clear that other metals, such as gold or nickel, may also be used in place of copper for plating the various vias and pads. The process for applying these metals is the same as that used for applying copper.

Claims 12 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobs (U.S. Patent # 6,294,407 B1) in view of Shih et al. (U.S. Patent # 6,286,208 B1).

Jacobs show the features of the claimed invention as detailed above, but fail to explicitly show support posts positioned adjacent the interposer structure, wherein the support posts support a heat spreader over the semiconductor chip.

Shin et al. is cited for showing interconnection with contact pads having enhanced durability. Specifically, Shih et al. (figures 1 to 21) specifically figure 9 show a semiconductor module **59**, comprising: a semiconductor chip **30**; a substrate **65**; and an interposer structure **10** electrically connecting the semiconductor chip to the substrate, wherein the interposer structure includes metallurgical **22** through connections having a predetermined shape and further comprises support posts **56** positioned adjacent the interposer structure, wherein the support posts **56** support a heat spreader **55** over the semiconductor chip for the purpose of providing an improved electrical connecting device.

12. The semiconductor module of claim 10, Shih et al. further comprises support posts **56** positioned adjacent the interposer structure for supporting a heat spreader **55** over the semiconductor chip.

19. The method of claim 16, Shih et al. further comprising positioning support posts **56** adjacent the interposer structure to support a heat spreader **55** over the semiconductor chip.

Therefore, it would be obvious to one of ordinary skill in the art to use Shih et al.'s structure to modify Jacobs' structure for the purpose of providing an improved electrical connecting device.

Claims 12 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pierson et al. (U.S. Patent # 6,774,315 B1) in view of Shih et al. (U.S. Patent # 6,286,208 B1).

Pierson et al. show the features of the claimed invention as detailed above, but fail to explicitly show support posts positioned adjacent the interposer structure, wherein the support posts support a heat spreader over the semiconductor chip.

Shin et al. is cited for showing interconnection with contact pads having enhanced durability. Specifically, Shih et al. (figures 1 to 21) specifically figure 9 show a semiconductor module **59**, comprising: a semiconductor chip **30**; a substrate **65**; and an interposer structure **10** electrically connecting the semiconductor chip to the substrate, wherein the interposer structure includes metallurgical **22** through connections having a predetermined shape and further comprises support posts **56** positioned adjacent the interposer structure, wherein the support posts **56** support a heat spreader **55** over the semiconductor chip for the purpose of providing an improved electrical connecting device.

12. The semiconductor module of claim 10, Shih et al. further comprises support posts **56** positioned adjacent the interposer structure for supporting a heat spreader **55** over the semiconductor chip.

19. The method of claim 16, Shih et al. further comprising positioning support posts **56** adjacent the interposer structure to support a heat spreader **55** over the semiconductor chip.

Therefore, it would be obvious to one of ordinary skill in the art to use Shih et al.'s structure to modify Pierson et al.'s structure for the purpose of providing an improved electrical connecting device.

Claims 4 and 5 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

# Response

Applicant's arguments filed 3/14/06 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The insertion of Applicant's additional claimed language, for example, "in claim 1, 10 and 16" cause for further search and consideration to make this action final.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. ∋ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. ∋ 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. ∋ 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

The listed references are cited as of interest to this application, but not applied at this time.

| Field of Search | Date |
|---|---|
| U.S. Class and subclass:<br>257/712,713,713,717,720,704,710,675,773,774,778,734,737,738,780,e23.067,e23.101,e23.194,e21.503,e23.067<br>324/754,758,757,765,<br>174/255,256,260,261<br>361/748,760,761,762,767,769,771<br>439/65,66,91 | 12/11/05<br>5/19/06 |
| Other Documentation:<br>foreign patents and literature in<br>257/712,713,713,717,720,704,710,675,773,774,778,734,737,738,780,e23.067,e23.101,e23.194,e21.503,e23.067<br>324/754,758,757,765,<br>174/255,256,260,261<br>361/748,760,761,762,767,769,771<br>439/65,66,91 | 12/11/05<br>5/19/06 |
| Electronic data base(s):<br>U.S. Patents EAST | 12/11/05<br>5/19/06 |

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
5/21/06